WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a resistance layer formed on a semiconductor substrate of a first conductivity type and of a second conductivity type, one end of said resistance layer being adapted to have a first voltage applied thereto, another end of said resistance layer being adapted to have a second voltage applied thereto;

an oxide film formed on the resistance layer; and

a resistance bias electrode layer comprising a silicon layer formed on the oxide film;

wherein the device is configured so that voltage dependence of a resistance of the resistance layer is reduced by adjusting the voltage applied to the resistance bias electrode layer.

2. The semiconductor device of claim 1, wherein the resistance bias electrode is formed by depositing two silicon layers.

3. The semiconductor device of claim 1, wherein the voltage applied to the silicon layer is provided from the middle of the resistance layer in a lateral direction.

4. The semiconductor device of claim 1, 2 or 3, further comprising a pair of electrode pad layers of the second conductivity type formed at both ends of the resistance layer of the second conductivity type, wherein the voltage is applied to the electrode pad layers to provide the resistance layer with electric current.

5. The semiconductor device of claim 4, wherein the ratio of the voltage applied to the pair of the electrode pad layers to the voltage applied to the resistance bias layer is 0.5-0.6.

6. A method of manufacturing a semiconductor device, comprising:

forming an oxide film and a first silicon layer on a semiconductor substrate of a first conductivity type;

selectively forming an oxidation resistance film on the first silicon layer;

forming a field oxide film by thermal oxidation;

removing the oxidation resistance film;

forming a resistance layer of a second conductivity type on the surface of the semiconductor substrate by ion implantation of an impurity of the second conductivity type piercing through the first silicon layer and the oxide film;

forming a second silicon layer covering the whole area of the device;

forming a resistance bias electrode layer on the resistance layer through a patterning of the first and second silicon layers; and

forming a wiring layer for providing the resistance bias electrode layer with a predetermined voltage.

7. The method of manufacturing the semiconductor device of claim 6, wherein both of the silicon layers are made of polysilicon or amorphous silicon.

8. The method of manufacturing the semiconductor device of claim 6 or 7, wherein the oxidation resistance film is a silicon nitride film.

9. The method of manufacturing the semiconductor device of claim 6, wherein the wiring layer contacts with the resistance layer at the middle of the resistance layer in lateral direction.

10. A method of manufacturing a semiconductor device having a MOS transistor and a resistor element on a semiconductor substrate comprising:

forming an oxide film and a first silicon layer on a semiconductor substrate of a first conductivity type;

selectively forming an oxidation resistance film on the first silicon layer over both of a MOS transistor forming region and a resistance forming region;

forming a field oxide film by thermal oxidation;

removing the oxidation resistance film;

forming a resistance layer of a second conductivity type on the surface of the semiconductor substrate by ion implantation of an impurity of the second conductivity type piercing through the first silicon layer and the oxide film on the resistance forming region;

forming a second silicon layer covering the whole area of the device;

forming a resistance bias electrode layer on the resistance layer through the patterning of the first and second silicon layers and simultaneously forming the gate electrode of the MOS transistor;

forming simultaneously a source layer and a drain layer of the MOS transistor and a pair of electrode pad layers of the resistance layer; and

forming a wiring layer for providing the resistance bias electrode layer with a predetermined voltage.

11. The method of manufacturing the semiconductor device of claim 10, wherein the silicon layers are made of polysilicon or amorphous silicon.

12. The method of manufacturing the semiconductor device of claim 10 or 11 wherein the oxidation resistance film is a silicon nitride film.

13. The method of manufacturing the semiconductor device of claim 10, wherein the wiring layer contacts with the resistance layer at the middle of the resistance layer in lateral direction.